

## CLAIMS

What is claimed is:

1. A threshold-adjusted transistor, comprising:  
a substrate including:  
spaced-apart source and drain regions formed in the substrate;  
channel region defined between the source and drain regions;  
a layer of gate oxide formed over at least a part of the channel region; and  
a gate formed over the gate oxide, the gate further having at least one implant aperture formed therein, the channel region of the substrate further including an channel internal implanted region between the source and drain regions.
2. The transistor of claim 1, the substrate further comprising at least one lightly-doped structure located between at least one of the source and drain region and the channel region.
3. The transistor of claim 2, further comprising a double-diffused structure at least partially surrounding each of the channel internal implanted region and the at least one lightly-doped structure.
4. The transistor of claim 3, wherein the double-diffused structure is implanted at a diagonal angle to the gate and through the aperture of the gate.
5. The transistor of claim 1, the substrate further comprising an enhancement region located within at least a portion of the channel region.
6. The transistor of claim 2, wherein the channel internal implanted region and the lightly-doped structure are formed according to the same fabrication process.
7. The transistor of claim 2, wherein the lightly-doped structure is a lightly-doped drain (LDD) structure arranged between one of the drain and source regions and the channel region.

8. The transistor of claim 1, wherein the at least one implant aperture comprises a plurality of implant apertures arranged in a checkerboard configuration along the gate.

9. The transistor of claim 1, wherein the at least one implant aperture comprises a plurality of implant apertures arranged in a two dimensional array configuration along the gate.

10. A method for forming a transistor, comprising:  
forming a gate having source and drain ends and insulated from a substrate, the gate including at least one aperture extending therethrough to the substrate;  
forming doped regions in the substrate adjacent to the drain and source ends as separated by a channel region and in the substrate below the aperture of the gate; and  
forming source and drain regions in the substrate adjacent to the source and drain ends of the gate.

11. The method of claim 10, further comprising forming at least one lightly-doped structure located between at least one of the source and drain regions and the channel region.

12. The method of claim 11, further comprising forming a double-diffused structure at least partially surrounding each of the doped regions below the aperture of the gate and the at least one lightly-doped structure.

13. The method of claim 12, further comprising implanting the double-diffused structure at a diagonal angle to the gate and through the aperture of the gate.

14. The method of claim 10, further comprising forming an enhancement region in the substrate located within at least a portion of the channel region.

15. The method of claim 10, further comprising forming the doped regions according to a single fabrication process.

16. The method of claim 11, further including forming the lightly-doped structure as a lightly-doped drain (LDD) structure arranged between one of the drain and source regions and the channel region.

17. The method of claim 10, wherein the at least one aperture comprises a plurality of apertures arranged in a checkerboard configuration along the gate.

18. The method of claim 10, wherein the at least one aperture comprises a plurality of apertures arranged in a two dimensional array configuration along the gate.

19. In a fabrication process optimized for short-channel transistors, a method for adjusting a threshold voltage of a long-channel transistor, comprising:  
forming at least one aperture in a gate on a substrate;  
implanting a first dopant through the at least one aperture into a channel region of the substrate; and  
annealing the first dopant in the channel.

20. The method of claim 19, wherein the implanting and annealing the first dopant utilizes the implanting and annealing processes for forming lightly-doped drains of the short-channel transistors.

21. The method of claim 19, further comprising implanting a second dopant into the at least one aperture and annealing the second dopant to form a double-diffused structure at least partially surrounding the first dopant.

22. The method of claim 21, wherein the implanting of the second dopant occurs at an angle off-vertical through the at least one aperture of the gate.

23. The method of claim 19, wherein forming comprises arranging a plurality of apertures along the length of the gate.

24. The method of claim 23, wherein the apertures of the plurality are arranged in a checkerboard configuration along the gate.

25. The method of claim 23, wherein the apertures of the plurality are arranged in a two dimensional array configuration along the gate.

26. A method for manufacturing a MOS structure on a semiconductor substrate, comprising:  
forming a gate oxide layer over the semiconductor substrate;  
forming a polysilicon layer over the gate oxide layer;  
patterning and etching the first mask layer to form a gate having an aperture between source and drain ends in the polysilicon layer;  
forming implant regions in the substrate adjacent to the drain and source ends and within the aperture of the gate; and  
forming source and drain regions in the substrate adjacent to the source and drain ends of the gate.

27. The method of claim 26, wherein forming the implant regions comprises forming lightly-doped drain structures in the substrate.

28. The method of claim 27, wherein forming the implant regions further comprises forming double-diffused structures at least partially surrounding the lightly-doped drain structures.

29. The method of claim 28, further comprising implanting the double-diffused structure at a diagonal angle to the gate and through the aperture of the gate.